2011 8th International Multi-Conference on Systems, Signals & Devices

PARAMETERS EFFECT ON BASIC DC TO DC CONVERTER STRUCTURES

N. Ben Amor[1,2], O. Kanoun[2], N. Derbel[1]
[1]Research unit on Intelligent Control, design & Optimization of complex Systems (ICOS)
Sfax National School of Engineering BPW 3038- Tunisia
[2]Chair of Measurement and Sensor Technology, University of Chemnitz, Germany,
Tel: +49-(0)371-531 36931
Email: nidhal.ben.amor@ieee.org

ABSTRACT

Progress in low power Very Large Scale Integration (VLSI) design open up possibilities of powering wireless devises from scavenged ambient energy. An energy management system should be designed to manage the harvested energy. DC to DC converters represent the key element in energy management systems. Knowing the diversity of DC-DC converters generally designed for specific applications, basic converters are under scope in this paper. Operation principles and simulation patterns of basic DC to DC converters are first presented. Parameter simulation occurring the effect of duty cycle, inductance, capacity and switch polarisation is studied in depth. The gaol of this paper is to show main parameters effect on output voltage behaviour. Simulation results show that the main parameters in DC-DC converters design play a key role to avoid extra-lose of harvested energy.

Index Terms— energy harvesting, energy management, DC-DC converter

1. INTRODUCTION

DC-DC conversion is the key element in energy management systems [1, 2]. Showing a wide diversity depending on their structure, energy consumption, response times, etc.. [3, 4, 5], The DC-DC converters are ubiquitous in these systems. Indeed, the new DC-DC converters have a certain degree of complexity [6, 7]. This paper investigates the effects of parameter changes on the different basic structures of these converters. Boost, buck and buck-Boost converters represent the basic structures of the DC-DC conversion.

Based on a switching mode with at least two semiconductor switches (a transistor and a diode) and a storage unit, the role of these basic structures is respectively to increase, to reduce or to increase and to reduce a direct voltage input.

For the whole structures the input power can come from DC sources such as batteries, solar panels, rectifiers and DC generators [8, 9]. A boost converter (buck converter) is a DC to DC converter with an output voltage greater (lower) than the source voltage. A boost converter (boost converter) is also called a step-up (step-down) converter. Since power ($P = VI$) must be conserved, the output current is lower (higher) than the source current.

The buck–boost converter is a type of DC-DC converter that has an output voltage magnitude that is either greater than or less than the input voltage magnitude. It is a SMPS (Switching Mode Power Supply) with a similar circuit topology to the boost converter and the buck converter. The output voltage is adjustable based on the duty cycle of the switching transistor.

This paper studies the effect of several parameters affecting the behaviour of basing DC-DC converters. These parameters are mainly the structure (P-junction or N-junction) of the transistor used as switch in the circuit, values of inductance and capacity used in the converter circuit, obviously the duty cycle and the input voltage. The value of the input voltage V_{in} can influence the behaviour of the converter, however, this behaviour differs from one circuit to another (from one transistor to another). As a result, and since no rules that can be set for the V_{in} variation, its effect is excluded from this study.

Knowing that the majority of energy management systems seek to supply portable systems in constant voltage [10]; thus, this paper is interested in the voltage behaviour through a variation of the parameters mentioned above.

2. SIMULATION PARAMETERS

General conditions of simulations are set for different tests. The input voltage is set at V_{in} = 5V. The inductance and capacitance of the circuit are fixed respectively at L = 10 mH and C = 1 µF. Output resistance (system load) R = 3.3 KΩ. A diode ref. D1N4002 (1A ; 100V). A duty cycle D = 50 %. MOS transistors acting as switches: A PMOS transistor ref. M2N6849 and a NMOS transistor ref. IRF150; the rational aspect of both transistors is W / L (100 µ / 2 µ).

Figures 1, 2 and 3 show the simulations patterns (using a PMOS transistor) of boost, buck and buck-boost converters respectively.

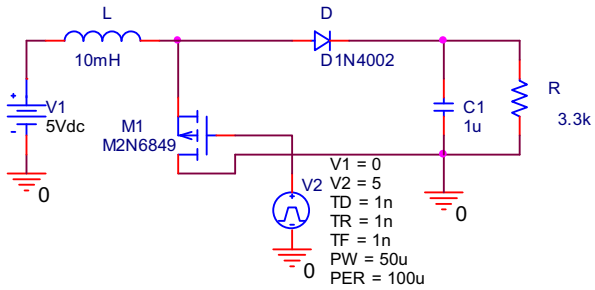

Figure 1. Boost converter simulation pattern

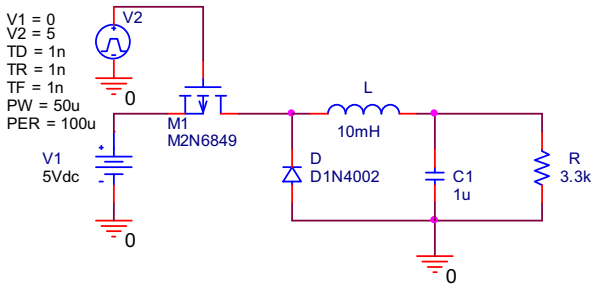

Figure 2. Buck converter simulation pattern

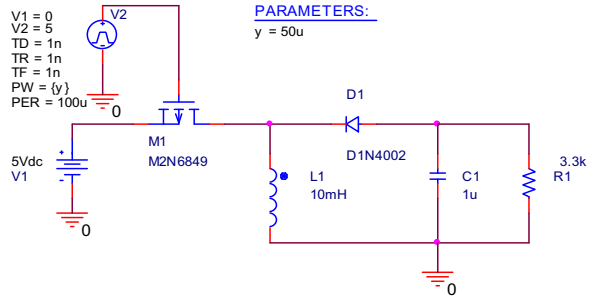

Figure 3. Buck-boost converter simulation pattern

The following paragraphs discuss the effect of variation of each parameter on the behaviour of the converter circuit while keeping other parameters fixed.

3. DUTY CYCLE EFFECT

For a variation of the duty cycle from 10% to 100% (the switch is ON), the boost circuit has two behaviours. The first, for duty cycles D ≥ 80%, is a buck behaviour contrary to the proper functioning of the circuit: output voltages are lower then input voltages. The second is the suitable functioning of the circuit: the output voltages are higher than V_{in}. The duty cycles 50%, 60% and 70% provide better system stability. Lower is the duty cycle higher is V_{out} with a late reached stability.

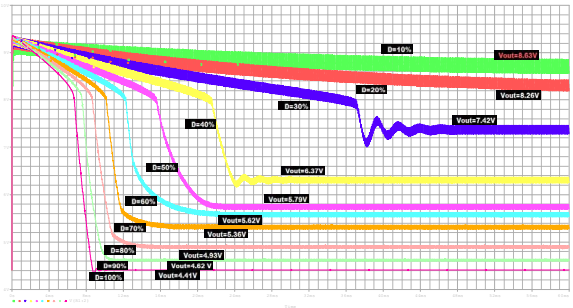

Figure 4. Duty cycle effect on Boost converter using PMOS switch.

For the buck converter, the same variation of the duty cycle gives the appropriate behaviour: the output voltages are less than V_{in}. For PMOS circuit the higher is D the lower is the voltage (V_{out} = 0V for D = 100%). Unlike the PMOS circuit, the NMOS circuit generates voltage output that increases if D increases with a maximum for D = 70% (shown in figure 5). The duty cycles D = 80%, 90% and 100% generate an output voltage peak while remaining inferior to V_{in} to be stabilized thereafter.

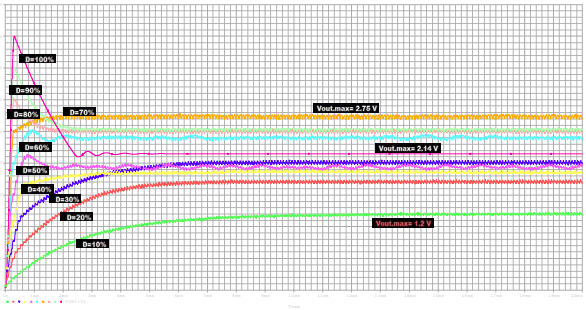

Figure 5. Duty cycle effect on Buck converter using NMOS switch.

The buck-boost converter generates voltages with an inversed polarity comparing with V_{in} polarity with higher and lower amplitudes. More the duty cycle increases more the system converges from boost behaviour to buck behaviour.

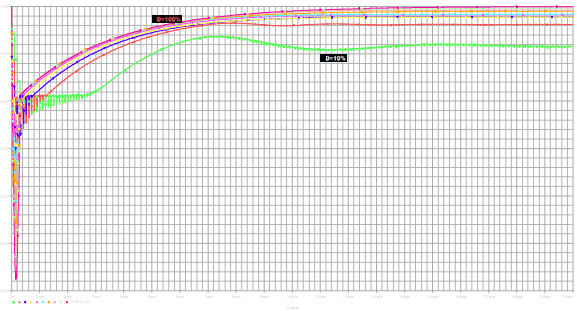

Figure 6. Duty cycle effect on Buck-Boost converter using PMOS switch.

4. INDUCTANCE VARIATION EFFECT

As shown in figure 7 (same for circuit using NMOS switch), more the value of the inductance increases the output voltage decreases. Circuits using NMOS switch generate voltages stabilized faster than those generated by circuits using PMOS switches.

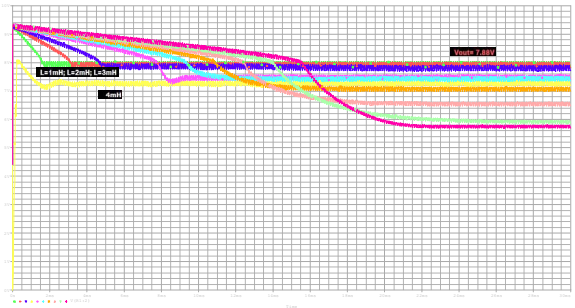

Figure 7. Inductance value effect on Boost converter using PMOS switch.

Same thing for buck converters, lower is the inductance higher is the output voltage. Like the boost converter, voltages generated by circuit using NMOS transistor are faster stabilised (as shown in figure 8) than those generated by circuit using PMOS.

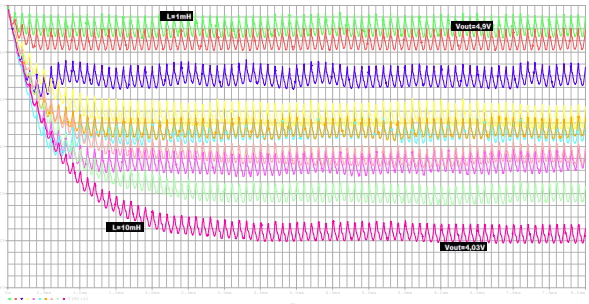

Figure 8. Inductance value effect on Buck converter using PMOS switch.

For buck-boost converter using NMOST, output voltages are faster stabilised. Absolut values of these voltages are near to each other for an inductance variation from 1 mH to 10 mH with 1 mH as a step.

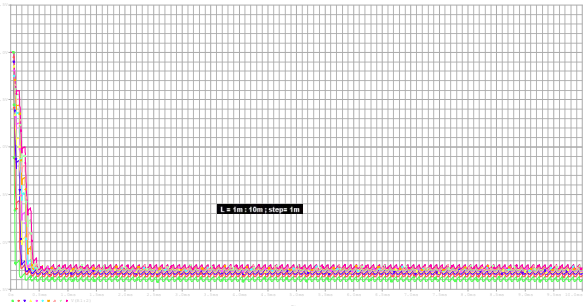

Figure 9. Inductance value effect on Buck-Boost converter using NMOS switch.

5. CAPACITY VARIATION EFFECT

As a general behaviour for all the converters, higher is the capacity higher is the output power. As a curve example, figure 10 shows voltage variation of buck-boost converter using PMOS switch.

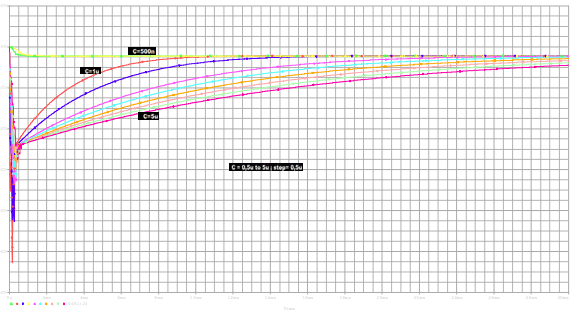

Figure 10. Capacity value effect on Buck-Boost converter using PMOS switch.

6. MOS SWITCH POLARISATION EFFECT

For the same parameters configuration, boost and buck converters show different aspect using both transistor technologies. With PMOS transistors, output voltage has tendency to decrease to stabilize. Voltages in circuits using NMOS transistors start from 0V to reach a peak before being stabilized.

It's to mention also, that time spent by voltages to be stabilized in NMOS circuits is shorter then time used in PMOS circuits.

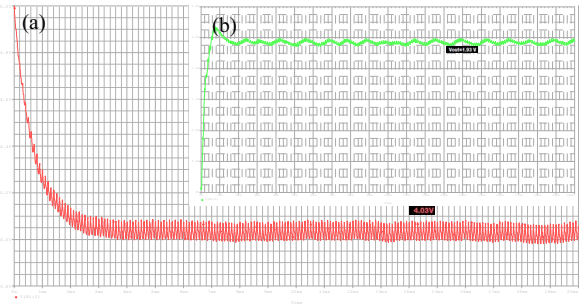

Figure 11. Buck converter simulation result. (a) using PMOST ; (b) using NMOST

CONCLUSION

For every new energy harvesting system, a dedicated DC-DC converter is designed. However, their functions derivate from basic DC-DC converters (Boost, Buck and Buck-Boost) we focused on in this paper. Our study investigates the behaviour of output voltage regarding influence of transistor polarisation (P or N), capacity, inductance and duty cycle.

Simulations show that output voltages in converters using PMOS transistors as a switch, have a tendency to

decrease before being stabilized. Using NMOST, offer an output voltages starting from zero to reach a peak first, then to stabilize in a final value during a period lower than needed in converters using PMOST. Thus, for applications giving more importance to time than energy consumption, it's advised to use NMOST as a switch (reaching a peak of power, NMOS circuits consume more energy).

Capacity plays a role of energy tank in such converters. Simulations confirm that higher is the capacity higher is the output voltage.

Accordance with the power law in an inductance, results show that higher is the inductance lower is the output voltages.

Simulations demonstrate also that boost converters should not have high duty cycles, which is the case for new wireless computing devises. Better system stability can be reached for medium duty cycles (from 50% to 70%). In applications using buck converters, duty cycle values should be taken into account simultaneously with transistor polarisation. Indeed, in PMOS (-- NMOS --) circuit, higher is the duty cycle lower (-- higher --) is the output voltage.

Buck-Boost converters are more useful in energy harvesting applications offering an ambient energy sources with voltage variation (ΔV up to 5V) such as solar cell energy. In those applications, the Buck-Boost converter converges from boost to buck behaviour as well as duty cycle increases.

ACKNOWLEDGEMENTS

The authors would like to acknowledge the German Academic Exchange Service (DAAD) for mobility scholarships.

REFERENCES

[1] A. Kansal, J. Hsu, S. Zahedi and M. Srivastava, "Power management in energy harvesting sensor networks," *Transactions on Embedded Computing Systems*, vol. 6, no. 4, pp. 1-32, 2007.

[2] A. Kansal, D. Potter and M. Srivastava, "Performance aware tasking for environmentally powered sensor network," in proc. of *the International Conference on Measurements and Modelling of Computer Systems*, New York, USA, June 10-14 2004, pp. 223-234.

[3] T. Voigt, A. Dunkels, J. Alonso, H. Ritter, J. Schiller, "Solar-aware clustering in wireless sensor networks," in *Proc. of the 9th IEEE Symposium on Computers and Communications,* June 2004, vol. 1, pp. 238-243.

[4] C. Park and P.H. Chou, "Ambimax: Autonomous energy harvesting platform for multi-supply wireless sensor nodes," in *Proc. of the Sensor and Ad Hoc Communications and Networks SECON'06*, Vol. 1, 2006.

[5] J. Hsu, S. Zahedi, A. Kansal, M. Srivastava and V. Raghunathan, "Adaptive duty cycling for energy harvesting systems," in *Proc. of the 2006 international symposium on low power electronics and design*, New York, USA, pp. 180-185.

[6] C.M. Vigorito, D. Ganesan and A. G. Barto, " Adaptive Control of duty cycling in energy-harvesting wireless sensor networks," in *4th Annual IEEE Communications Society Conference on Sensor, Mesh and Ad Hoc Communications and Networks (SECON 2007)*, San Diego, CA, June 2007, pp. 21-30.

[7] K. Roemer and F. Mattern, "The design space of wireless sensor networks," in *IEEE Wireless Communications*, vol. 11, December 2004, pp. 54-61.

[8] V. Raghunathan, A. Kansal, J. Hsu, J. friedman and M. Srivastava, "Design considerations for solar energy harvesting wireless embedded ystems," in *Proc. of the 4th International Symposuim on Information Processing in Sensor Networks*, Los Angeles, California, USA, April 25-27 2005, pp. 457-462.

[9] F. Simjee and P.H. Chou, "Everlast: long-life supercapacitor-operated wireless sensor node," in *Proc. of the 2006 International symposium on low power electronics and design*, New York, USA, 2006, pp. 197-202.

[10] J-J. Chen and T-W. Kuo, "Voltage-scaling scheduling for periodic real-time tasks in reward maximization," in *the 26th IEEE Real-Time Systems Symposium (RTSS)*, Miami Florida, USA, December 5-8 2005, pp. 345-355.